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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,934	08/08/2001	Matthew C. Mattina	1662-38300 JMH (P01-3570)	3940

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EXAMINER	
ANYA, CHARLES E	

ART UNIT	PAPER NUMBER
2194	

MAIL DATE	DELIVERY MODE
10/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/924,934	MATTINA ET AL.	
	Examiner	Art Unit	
	Charles E. Anya	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *18 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18,19,21-26 and 28-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,13-16,18,19,21,22,24-26 and 28-31* is/are rejected.

7)☐ Claim(s) *6,10-12,23 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

WILLIAM THOMSON
SUPERVISORY PATENT EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16,18,19,21-26 and 28-34 are pending in this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,13,16 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,185,658 B1 to Arimilli et al.

3. As to claim 1, Hagersten teaches a distributed multiprocessing computer system, which includes a plurality of processors each coupled to an associated memory module, wherein each associated memory module may store data that is shared between said processors (figures 1-2), said system comprising: a Home processor that includes a memory block and a directory for said memory block in an associated memory module (Home Node/SMP 12 (Directory 66/Memory 22) Col. 7 Ln. 6 – 61, figure 2 Col. 10 Ln. 59 – 67, Col. 14 Ln. 13 – 24); an Owner processor that includes a cache memory (Requesting Node/SMP12 (External Caches 18) Col. 7 Ln. 6 – 47, Col. 8 Ln. 10 – 29), and wherein said Owner processor obtains an exclusive copy of said memory block,

and stores said exclusive copy of said memory block in said cache memory ("...cache data..." Col. 9 Ln. 18 – 25, Col. 9 Ln. 54 – 57, "...read/write..." Col. 13 Ln. 21 – 30, "When clear...not written the updated copy..." Col. 15 Ln. 33 – 39); and wherein said Owner processor may displace the exclusive copy of said memory block, and return said displaced copy of said memory block to said Home processor ("Write back..." Col. 15 Ln. 32 – 36, Col. 24 Ln. 11 – 16) with a signal indicating that said Owner processor remains a sharer of said memory block ("...discarded...shared state...without acquiring the owned state..." Col. 13 Ln. 21 – 39, "...write stream transaction to a shared..." Col. 24 Ln. 16 – 23).

Hagersten is silent with reference to wherein when said Owner processor displaces said exclusive copy of said memory block, said Owner processor compares an address of any displaced memory block with an address of any memory block for which an exclusive resides in said Owner processor.

Arimilli teaches when said Owner processor displaces said exclusive copy of said memory block, said Owner processor compares an address of any displaced memory block with an address of any memory block for which an exclusive resides in said Owner processor ("...comparing a requested address with..." Col. 5 Ln. 62 – 67, Col. 6 Ln. 1 – 22, Col. 9 Ln. 30 – 35, Col. 10 Ln. 1 – 7).

It would have been obvious to one of ordinary skill in the art at the time invention was made to modify the system of Hagersten with the teaching of Arimilli because the teaching of Arimilli would improve the system of Hagersten by providing a victim

selection mechanism for efficiently selecting a cache line for deallocation (Arimilli Col. 6 Ln. 20 – 22).

4. As to claims 13 and 24, see the rejection of claim 1 above.

5. As to claim 16, Hagersten teaches the method of claim 13, wherein the act of updating the coherence directory includes modifying a register to indicate that the Owner processor has an exclusive copy of the memory block ("...updates..." Col. 19 Ln. 28 – 30).

6. Claims 2-5,7,8,14,15,18,19,21,22,25,26,28,29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,185,658 B1 to Arimilli et al. as applied to claims 1,13 or 24 above, and further in view of U.S. Pat. No. 6,141,734 B1 to Razdan et al.

7. As to claim 2, Hagersten teaches the directory associated with the Home processor indicates that said Owner processor has obtained exclusive control of said memory block (Directory 66 Col. 19 Ln. 15 – 34).

Arimilli and Hagersten are silent with reference to the distributed multiprocessing computer system of claim 1, wherein said Owner processor obtains an exclusive copy of said memory block by issuing a Load Lock instruction.

Razdan teaches the distributed multiprocessing computer system of claim 1, wherein said Owner processor obtains an exclusive copy of said memory block by issuing a Load Lock instruction (Col. 4 Ln. 38 – 55).

It would have been obvious to one of ordinary skill in the art at the time invention was made to modify the system of Arimilli and Hagersten with the teaching of Razdan because the teaching of Razdan would improve the system of Arimilli and Hagersten by allowing for techniques to streamline processing within the CPU, while at the same time attempting to reduce the total number of memory accesses.

8. As to claim 3, Hagersten teaches the distributed multiprocessing computer system of claim 2, wherein said Owner processor is capable of executing multiple threads concurrently (the sharer state indicates that more than one slave agent 104/home agent 102 could access the same memory at the same time, which in essence means that multiple slave agent 104/home agent 102 of each SMP node 12A-D would be executing parallel/concurrently), and may displace data associated with a non-executing thread from its associated cache memory ("...discarded..." Col. 13 Ln. 21 – 39).

9. As to claim 4, Arimilli teaches the distributed multiprocessing computer system of claim 3, wherein said Owner processor includes a register in which, an address is stored representing the memory block obtained in response to the Load Lock instruction, and wherein said Owner processor compares the address of any displaced

data with the address stored in said register ("...comparing a requested address with..." Col. 5 Ln. 62 – 67, Col. 6 Ln. 1 – 22, Col. 9 Ln. 30 – 35, Col. 10 Ln. 1 – 7).

10. As to clam 5, Arimilli teaches the distributed multiprocessing computer system of claim 4, wherein the Owner processor asserts a Victim To Shared message if the address of any displaced data matches the address stored in said register ("...assigning...cache coherency states..." Col. 5 Ln. 62 – 67, Col. 6 Ln. 1 – 22, Col. 9 Ln. 30 – 35, Col. 10 Ln. 1 – 7).

11. As to claim 7, Arimilli teaches the distributed multiprocessing computer system of claim 5, wherein the directory associated with the Home processor indicates that said Owner processor has become a sharer of said memory block in response to said Victim To Shared message ("...assigning...cache coherency states..." Col. 5 Ln. 62 – 67, Col. 6 Ln. 1 – 22, Col. 9 Ln. 30 – 35, Col. 10 Ln. 1 – 7).

12. As to claim 8, Hagersten teaches the distributed multiprocessing computer system of claim 7, wherein said Owner processor subsequently re-obtains an exclusive copy of said memory block to complete execution of the non-executing thread ("...without acquiring the owned state..." Col. 13 Ln. 39 – 42).

13. As to claims 14,15 and 25, see the rejection of claim 2 above.

14. As to claim 18, see rejection of claims 5 and 7 above.

15. As to claim 19, Hagersten teaches the method of claim 18, further comprising the act of updating the coherence directory to indicate that said Owner processor has become a sharer of said memory block in response to said Victim to Shares message ("...shared state..." Col. 13 Ln. 39 – 40).

16. As to claim 21, see the rejection of claims 1,5 and 19 above.

17. As to claim 22, Hagersten teaches the method of claim 21, wherein the Home processor invalidates all other shares when it sends an exclusive copy to the memory block to the Owner processor ("...owned..." Col. 13 Ln. 23 – 30).

18. As to claims 26,28,29 and 30, see the rejection of claims 3,5,7 and 8 respectively.

19. **Claims 9 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,887,138 to Hagersten et al. in view of U.S. Pat. No. 6,185,658 B1 to Arimilli et al. and further in view of U.S. Pat. No. 6,141,734 B1 to Razdan et al. as applied to claims 8 or 24 above, and further in view of U.S. Pat. No. 6,266,744 B1 to Hughes et al.**

20. As to claim 9, Razdan, Arimilli and Hagersten are silent with reference to the distributed multiprocessing computer system of claim 8, wherein the Owner processor asserts a Read-with-Modify Intent Store Conditional instruction to the Home directory to again request an exclusive copy of said memory block.

Hughes teaches the distributed multiprocessing computer system of claim 8, wherein the Owner processor asserts a Read-with-Modify Intent Store Conditional instruction to the Home directory to again request an exclusive copy of said memory block ("...read with modify..." Col. 42 Ln. 47 – 58).

It would have been obvious to one of ordinary skill in the art at the time invention was made to modify the system of Razdan, Arimilli and Hagersten with the teaching of Hughes because the teaching of Hughes would improve the system of Razdan, Arimilli and Hagersten by avoiding deadlock in multiprocessor systems for cases in which two or more processors are attempting to obtain ownership of a particular cache (Hughes Col. 39 Ln. 36 – 43).

21. As to claim 31, see the rejection of claim 9 above.

Allowable Subject Matter

Claims 6,10-12,23 and 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Response to Arguments

Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,748,498 B2 to Gharachorloo et al.: directed to executing cache coherence protocol in a plurality of processor nodes.

U.S. Pat. No. 6,108,764 to Baumgartner et al.: directed to concurrent access to multiple caches in plural processor systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles E. Anya whose telephone number is 571-272-3757. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Thomson can be reached on 571-272-3718. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

cea.

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